FAIRCHILD SEMICONDUCTOR™

March 1997

NM93C13/C14
256-/1024-Bit Serial EEPROM

General Description

The NM93C13/C14 is 256/1024, respectively, bits of CMOS electrically erasable memory divided into 16/64 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high speed, high reliability and low power. The NM93C13/C14 is available in an 8-pin SO package to save board space.

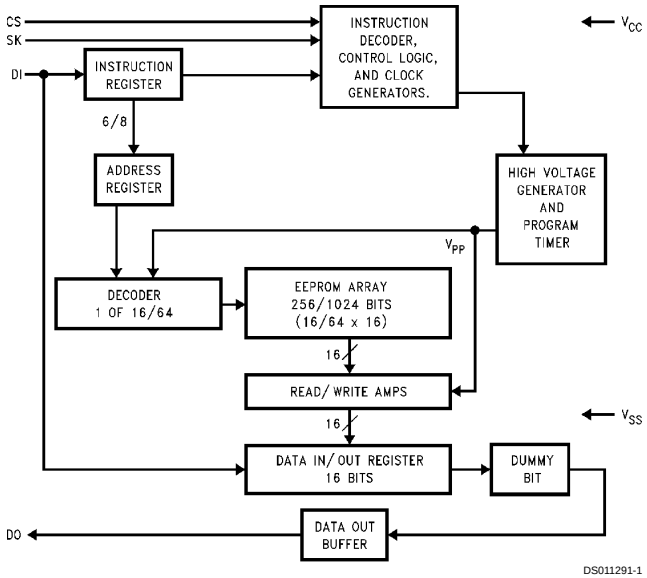
The serial interface of the NM93C13/C14 is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable.

All programming cycles are completely self-timed for simplified operation. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Typical active current 400 µA; Typical standby current 25 µA
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 15 years data retention
- Endurance: 100,000 read/write cycles minimum
- Packages available: 8-pin DIP, 8-pin SO

Functional Diagram



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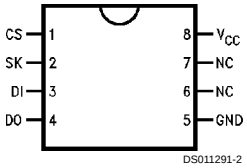
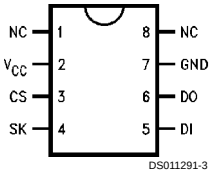
Connection Diagrams

Dual-In-Line Package (N)
and 8-Pin SO (M8)



Top View
See Package Number 8E and M08A
Alternate SO Pinout (TM8)
NM93C14 Only

Alternate SO Pinout (TM8)
NM93C14 Only



See Package M08A

Ordering Information

Commercial Temp. Range (0˚C to +70˚C)

Order Number*
NM93C13N/NM93C14N
NM93C13M8/NM93C14M8
NM93C14TM8

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	−65˚C to +150˚C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300˚C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C13–NM93C14	0˚C to +70˚C
Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics (Note 2)

V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current	CS = V_{IH}, SK = 1 MHz		4	mA
I_{CC3}	Standby Current	CS = 0V		200	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}	−10	10	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}	−10	10	µA
V_{IL}	Input Low Voltage		−0.1	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 1	
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −400 µA	2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = −10 µA	V_{CC} − 0.2		
f_{SK}	SK Clock Frequency			1	MHz
t_{SKH}	SK High Time	(Note 3)	300		ns
t_{SKL}	SK Low Time	(Note 3)	250		ns
t_{SKS}	SK Setup Time		50		ns
t_{CS}	Minimum CS Low Time		250		ns
t_{CSS}	CS Setup Time		50		ns
t_{DH}	D0 Hold Time		70		ns
t_{DIS}	DI Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{DIH}	DI Hold Time		20		ns
t_{PD1}	Output Delay to “1”			500	ns
t_{PD0}	Output Delay to “0”			500	ns
t_{SV}	CS to Status Valid			500	ns
t_{DF}	CS to DO in TRI-STATE®	CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time			10	ms

Capacitance (Note 4)

T_A = 25˚C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: 100% functional test; AC/DC parameters sample tested to 0.4% AQL.

Note 3: The SK frequency specification specifies a minimum SK clock period of 1 µs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 µs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 500 ns in order to meet the SK frequency specification.

Note 4: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C13/C14 have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C13 and C14 the next 8 bits carry the op code and the 6-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 500 ns (t_{CS}). DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 500 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 500 ns (t_{CS}). The ERASE ALL instruction is not required, see (Note 5) .

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 500 ns (t_{CS}).

Erase/Write Disable (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Note 5: The NM93C13/C14 devices do not require an "ERASE" or "ERASE ALL" prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with the NMOS NMC9346.

Instruction Set for the NM93C13 and NM93C14

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase selected register.
WRITE	1	01	A5–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

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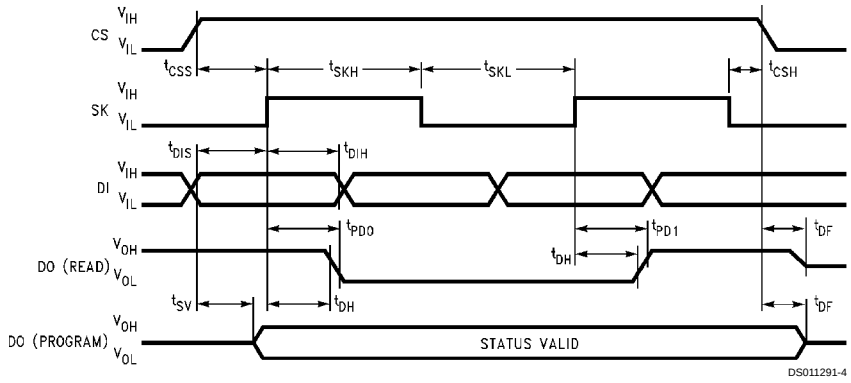
Timing Diagrams

Synchronous Data Timing



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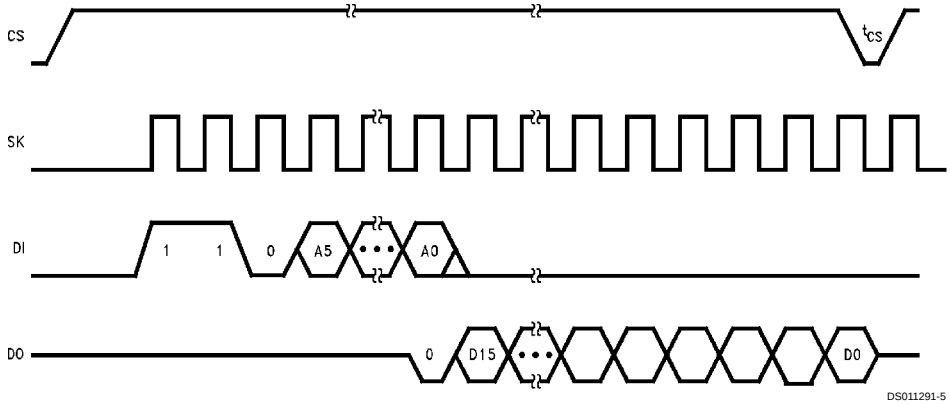
READ:



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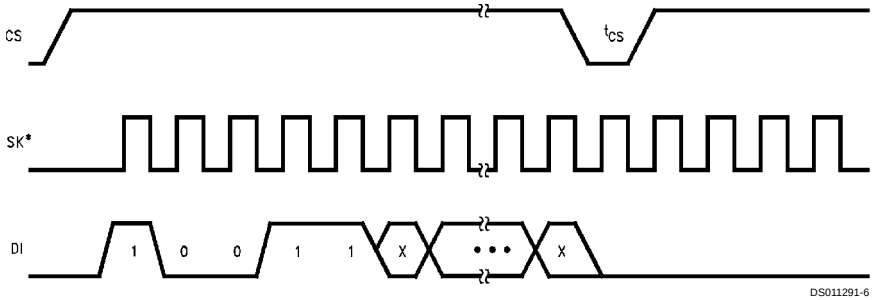
*Address bits A5 and A4 become “don’t care” for NM93C13.

EWEN:



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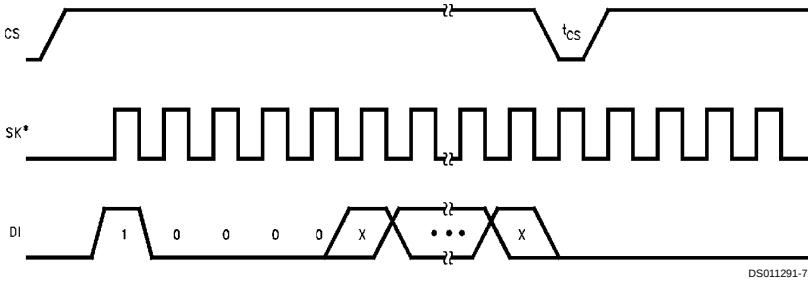
*The NM93C13 and NM93C14 require a minimum of 9 clock cycles.

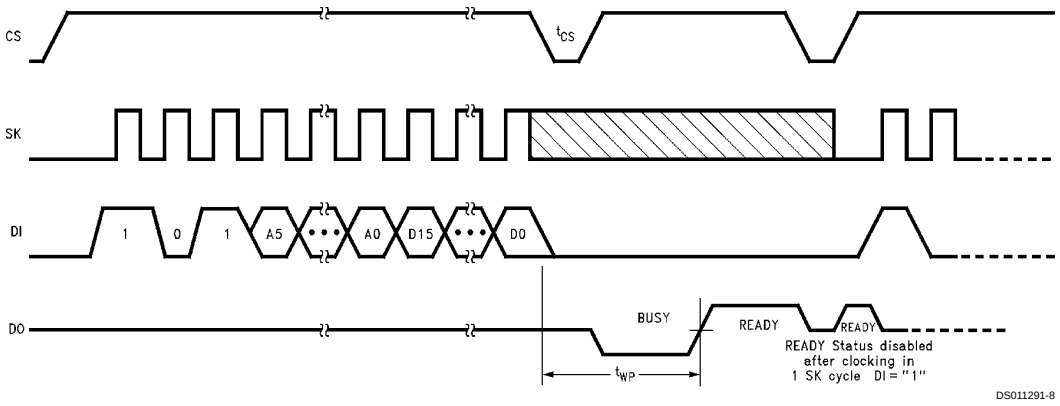
Timing Diagrams (Continued)

EWDS:



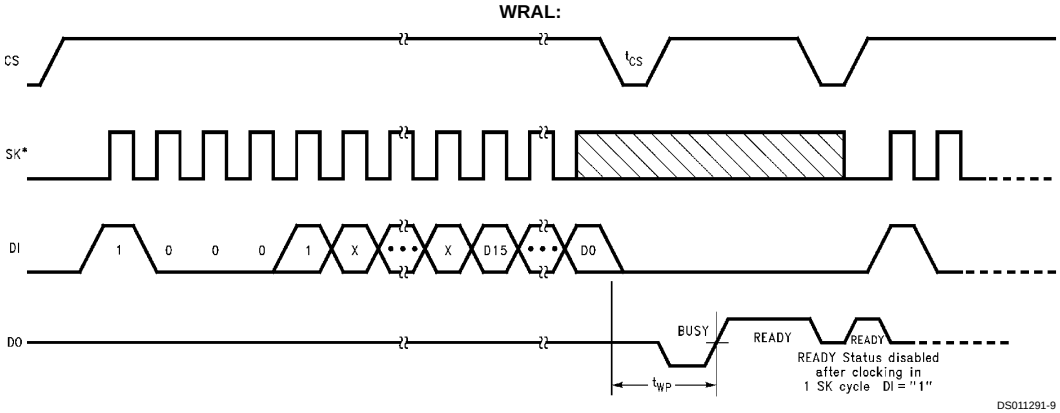
*The NM93C13 and NM93C14 require a minimum of 9 clock cycles.

WRITE:



*Address bit A5 and A4 become “don’t care” for NM93C13.

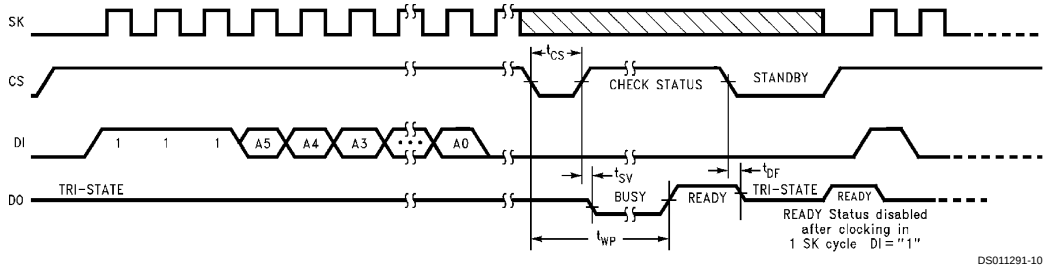
WRAL:



*The NM93C13 and NM93C14 require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

ERASE:



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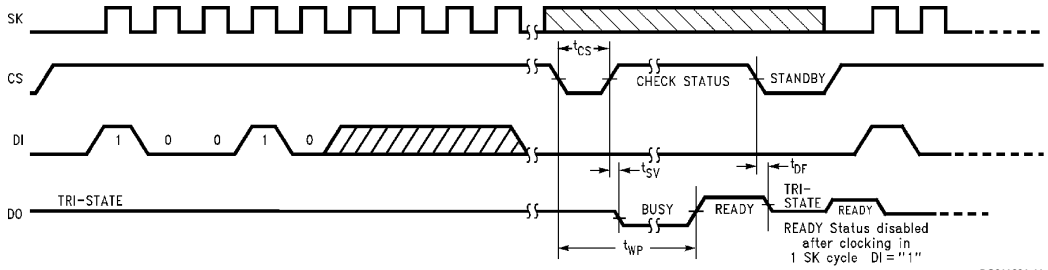
*Address bits A5 and A4 are "don't care" for NM93C13.

ERAL:



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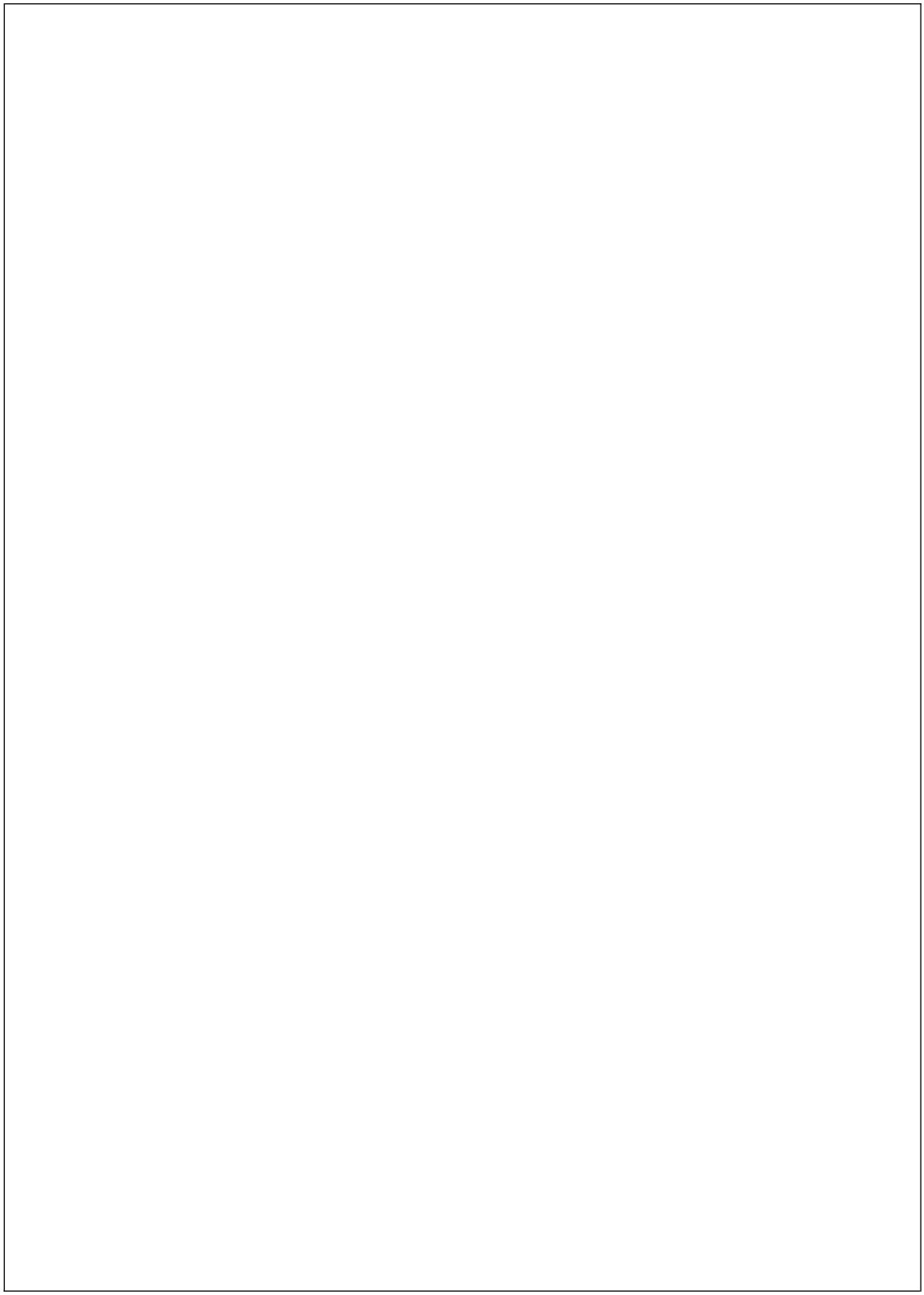
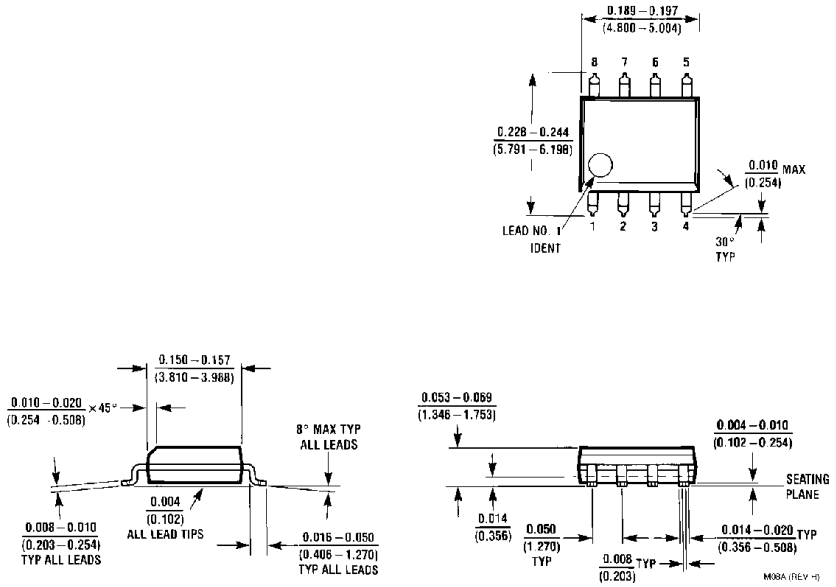
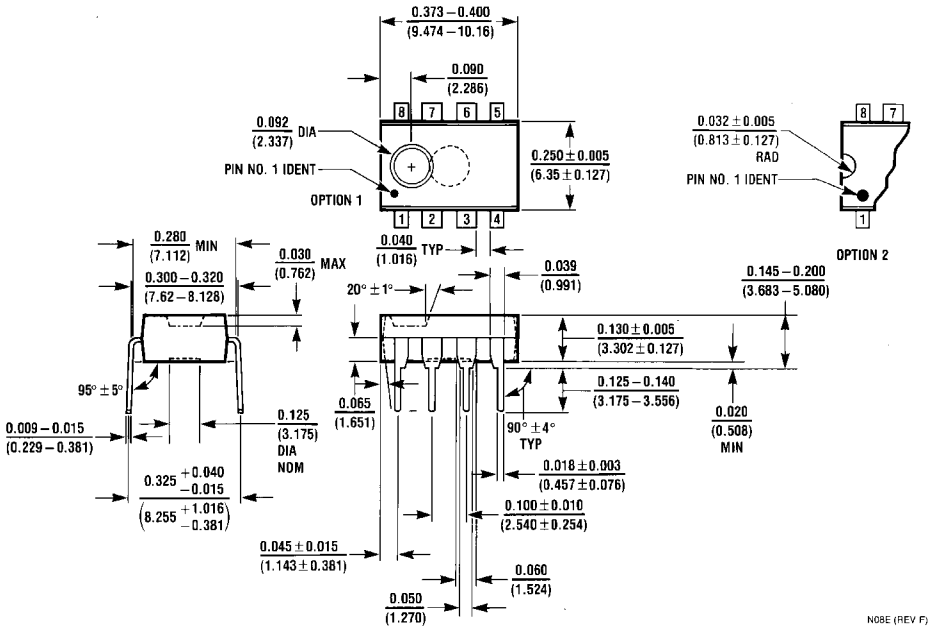


Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Order Number NM93C13M8 or NM93C14M8
Package Number M08A



Molded Dual-In-Line Package (N)
Order Number NM93C13N or NM93C14N
Package Number N08E

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